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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,734	04/17/2001	Takaaki Nagai	NECF 18.591	9062

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KATTEN MUCHIN ZAVIS ROSENMAN
575 MADISON AVENUE
NEW YORK, NY 10022-2585

EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,734	NAGAI, TAKAAKI	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 1, 2003 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 8 recites the limitation "...said tunneling gate oxide layer..." in lines 9 and 10. There is insufficient antecedent basis for this limitation in the claim. The scope of the claim is nebulous because the location of tunneling gate oxide layer cannot be determined, lacking any previous recitation of this limitation. Since the second semiconductor layer is prohibited from contacting the tunneling gate oxide layer in lines 8 and 9, the location of the tunneling oxide is necessary for determination of the scope of the claimed invention.

5. Lines 22 and 23 recite the limitation, "...an insulating layer...being used as a tunneling gate oxide layer...". The scope of the claim is vague because it is not known if this is a reference to the tunneling gate oxide layer mentioned in line 9 or if this is a second tunneling oxide layer.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2 and 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 5,445,983 to Hong in view of US patent No. 6,091,634 to Wong.

Regarding claim 1, Hong teaches a non-volatile semiconductor storage apparatus comprising:

a memory cell field effect transistor having a floating gate (42) and a control gate (46);

a select field effect transistor (24) having a drain (39) connected to a source of the memory cell field effect transistor;

said floating gate extending to a position above the gate of the select transistor, wherein top and bottom surfaces of the floating gate and the control gate are parallel to top and bottom surfaces of the gate of the select field effect transistor; and

a tunneling gate oxide layer (36) below the floating gate and the gate of the select transistor.

Hong does not teach an array of storage cells. Wong teaches an array of storage cells (Fig. 1). It would have been obvious to one of ordinary skill in the art to incorporate the array of memory cells taught by Wong into the device taught by Hong since it is necessary to form an array in order to make a useful memory device.

Regarding claim 2, Hong teaches a non-volatile semiconductor storage apparatus having a memory cell field effect transistor and a select field effect transistor, said memory cell field effect transistor having a floating gate (42) and a control gate (46), the select field effect transistor having a drain (39) connected to a source of the memory cell FET, said storage apparatus comprising:

a first semiconductor layer composing a portion of the floating gate and a gate of the select field effect transistor (the lower portion of the floating gate (42) is in the same layer of the device as the select gate (24);

an upper portion (second layer) of the floating gate (42) above a lower portion (first layer), said second portion not contacting the tunnel oxide, the upper portion (second layer) having a lower surface located at a height at least equal to a height of an upper surface of the lower portion (first layer), said second portion (second layer) extending to a position above the select gate (note: since the first and second layers comprise the same material, the only difference is in the method of production. Therefore, the floating gate of Hong can be split into portions and considered two layers);

a first insulation layer (41) which insulates the select gate from the floating gate, said first insulation layer contacting said first semiconductor layer;

a second insulation layer (45) formed on the second semiconductor layer (second portion);

a third semiconductor layer (46) on the second insulation layer and composing said control gate;

the third semiconductor layer, the second insulation layer, and the second semiconductor layer being etched using a single photoresist film (47; Fig. 3L); and

a tunnel gate oxide layer (36) below the floating gate and the select gate.

Hong does not teach an array of storage cells. Wong teaches an array of storage cells (Fig. 1). It would have been obvious to one of ordinary skill in the art to incorporate the array of memory cells taught by Wong into the device taught by Hong since it is necessary to form an array in order to make a useful memory device.

Regarding claims 5 and 6, Hong does not teach a drain diffusion layer shared between adjacent memory cell field effect transistors in a first direction in said unit cells. Wong teaches a drain diffusion layer shared between adjacent memory cell field effect transistors in a first direction in said unit cells. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Wong into the device taught by Hong for reasons discussed above.

Regarding claim 7, Hong teaches a non-volatile semiconductor storage apparatus comprising:

a memory cell field effect transistor having a floating gate (42) and a control gate (46);

a select field effect transistor (24) having a drain (39) connected to a source of the memory cell field effect transistor;

said floating gate extending to a position above the gate of the select transistor, wherein top and bottom surfaces of the floating gate and the control gate are parallel to top and bottom surfaces of the gate of the select field effect transistor; and

a tunneling gate oxide layer (36) below the floating gate and the gate of the select transistor.

Hong does not teach an apparatus comprising cell units in a rectangular matrix shape, a source line commonly connecting sources in one direction and a drain diffusion layer shared between adjacent memory cells in a second direction. Wong teaches each of these features (See Fig. 1, for example). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Wong into Hong for reasons discussed above.

Neither Hong nor Wong explicitly teach a semiconductor layer connecting the source and source line. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a semiconductor layer, since semiconductor material is commonly used in the art for the purpose of forming conductive line. It would have been further obvious to use a known material that is well suited for the intended use.

Response to Arguments

8. Applicant's arguments filed October 1, 2003 have been fully considered but they are not persuasive.

9. The Applicant argues that Hong does not teach an insulating layer below the floating gate and the gate of the select field effect transistor, wherein the insulating layer is used as a tunneling insulator. This teaching can be seen in Fig. 1A, for example, in Hong, where the tunneling insulator (36) is disposed below the floating gate (42) and the gate (24) of the select transistor. While the tunnel insulator is not directly beneath the select gate, the claims only require that the tunnel insulator be below the select gate and the floating gate. The tunnel insulator taught by Hong is disposed lower than both the floating gate and the select gate, hence it can be said that it is below both of them.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

DWO

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800